

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 11-224941
(43)Date of publication of application : 17.08.1999

(51)Int.Cl. H01L 27/146
H04N 9/07

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(30)Priority
Priority 97 960418 Priority 29.10.1997 Priority US
number : date : country :

(54) **MANUFACTURE OF ACTIVE PIXEL SENSOR HAVING PROGRAMMABLE
COLOR BALANCE**

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a programmable color balance which ensures efficient use of a silicon area and high signal-to-noise ratio(SN ratio).

SOLUTION: A pixel architecture 20 has a transfer gate bus for each color. For example a TGg bus 1 is connected to transfer gates 24 of green pixels in a column A and a TGr bus 2 is connected to transfer gates 24 of red pixels in the column A. Since the bus is provided for each color the time for which charges are stored in a PD 22 can be determined color by color. Since the color balance is obtained by such a method that depends on the charges to be stored in the PD 22 noise in the circuit can be reduced.

CLAIMS

[Claim(s)]

[Claim 1] Two or more pixels formed on main surfaces of a semiconductor substrate.

Two or more light filters which comprise at least two kinds arranged by said pixel of different colors and a

photodetector with which each aforementioned pixel contains sense nodes.

A step which provides two or more gates which have a control means which rectifies electrostatic potential close to said photodetector when it is a manufacturing method of an image sensor provided with the abovesaid photodetector is adjoined and a predetermined signal is impressed to a gateAre two or more buses arranged so that it may have at least one bus to each color of said different colorand the each via said control meansIt has a step which forms two or more buses which connect so that said gate and operation only relevant to one of said different color may coordinateand a step which controls said gate and sets up individual storage time to said different color.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention]This invention relates to a means to provide a color image sensor with a programmable color-balancemaintaining a high signal to noise ratio (signal to noise ratio) especially about the semiconductor photosensor and imager which are called an active pixel sensor (APS).

[0002]

[Description of the Prior Art]APS equipment is a semiconductor imager and each of that pixel usually includes a light sensing meansa resetting meansa charge transfer meansan electric charge-voltage converting means and the whole amplifieror a part. Each line or line in an imager is chosenand APS equipment operates by what is read using a line and a row selection signal (it is equivalent to the word and bit lines of a memory apparatus respectively).

[0003]The typical APS pixel of conventional technology is shown in drawing 1 and drawing 2. The photodetector (PDET) whose pixel of drawing 1 is either a photo-diode (PD) or a photogate (PG)It has a reset transistor including a transfer gate (TG)a floating diffusion region (FD)and a reset gate (RG)a line selection transistor containing a line selector gate (RSG)and a signal transistor (SIG). The pixel of drawing 2 generally has a photodetector (PDET) which is a photo-diode (PD)a reset transistor including a reset gate (RG)a line selection transistor containing a line selector gate (RSG)and a signal transistor (SIG). In

all the pixels of a conventional type in order to carry out easily above-mentioned line unit sensor mode reading. TG node, RG node and the RSG node in one pixel are connected by single bus assigned to the pixel single tier. Since the storage time of the pixel of drawing 1 is time until it operates after that and transmits an electric charge to FD from the time of the operation stop of TG being carried out and accumulation being started, the storage time of each pixel of the line is the same. In the pixel of drawing 2 which is time until a read signal is impressed and the electric charge in PD is read from the time of RG operating and PD being reset, the storage time of each pixel of a line has the same storage time similarly.

[0004] In conventional equipment, the image pick-up of each line is usually temporarily transposed to other lines and sequential execution of the image pick-up in each line is carried out. And each line has the same storage time. At the time of a color image pick-up, a color filter array (CFA) is applied to an image sensor. Each light filter of these usually pass the light energy of a different quantity and are entered in a sensor. An initial complement does not pass the light energy with which a light filter is originally demanded for a color-balance or the display purpose.

[0005]

[Problem to be solved by the invention] Therefore, a sensor output must carry out signal processing for a sensor output irrespective of an analog or digital one. By it, the suitable gain for each color channels is supplied and a desired color-balance is generated. In APS equipment, although signal processing of this voltage dependence can be carried out on a chip, it lists the fault by it to below.

[0006] (1) Induce a noise by a sensor.

[0007] (2) A complicated circuit is needed, consume more silicon area and electric power and reduce a frame rate.

[0008] If an example is taken in an above-mentioned situation, it will be clear that the APS equipment which improved the color-balance in conventional technology is needed.

[0009]

[Means for solving problem] This invention aims at solution of the above-mentioned problem by making a programmable color-balance feasible with a color image sensor, avoiding an above-mentioned fault. One approach which provides a programmable color-balance means by which signal processing of voltage dependence is not carried out is adjusting the storage time of each color. When it is carried out, the

signal charge generated in a pixel is proportional to a desired color-balance and subsequent processing does not have necessity. This invention provides the method of controlling accumulation individually also to which predetermined color. In that case the same sensor read-out mechanism is held and color-balance signal processing of the further required voltage dependence is made unnecessary in the equipment of conventional technology. The above becomes possible by establishing a separate transmission gate bus or a reset gate bus in each color in a predetermined line. Thus the storage time of each color of a predetermined line is controlled individually.

[0010] This invention is for solving one or more above-mentioned problems. Two or more pixels in which this invention is a semiconductor image sensor it is formed on the main surfaces of a semiconductor substrate and the each has a photodetector if it summarizes according to one mode of this invention. Two or more light filters which are arranged by said pixel and comprise at least two different colors and the transfer gate which approaches a photodetector and is controlled by one of two or more of the electrodes are included. If predetermined voltage is impressed to said electrode of a transfer gate the transfer gate will modulate the electrostatic potential close to a photodetector and will transmit electrostatic potential to sense nodes from a photodetector. A semiconductor image sensor includes two or more buses arranged so that at least one color bus may be further formed to each color of a different color. Each bus is connected so that the transfer gate and operation only relevant to one of a different color may coordinate via one of said the electrodes. A semiconductor image sensor has at least one connection to each color bus and includes again the timing circuit which can generate predetermined voltage to predetermined timing by bus. In this semiconductor image sensor the storage period controlled by a timing circuit regardless of other different colors can be set up to each different *****.

[0011] The point of providing a color-balance high [a signal to noise ratio (signal to noise ratio) with efficient use of silicon area] as an advantage of this invention and programmable is mentioned.

[0012] The above of this invention and other modes problem the feature and an advantage will be more clearly understood by referring to reading detailed explanation of following suitable embodiments and an accompanying drawing. The element common to two or more attached Drawings has attached the mark similar in the ability to do in order to

make it easy to understand.

[0013]

[Mode for carrying out the invention]The new pixel configuration of which the suitable embodiment of this invention conceives is shown in drawing 3drawing 4drawing 5and drawing 6. This invention is feasible at other physical embodiments. The Reason the embodiment shown in drawing 3drawing 4drawing 5and drawing 6 was chosen is that they are the embodiments optimal for this inventionas far as this invention person gets to know.

[0014]Each figure shown in drawing 3 and drawing 4 shows the array of four pixels which incorporated this invention to the sensor which has a pixel arranged so that a line and a sequence may be formed. In each figure of drawing 3 and drawing 4the pixel is arranged so that a quadrant may be formed. This quadrant comprises two lines containing two pixels. When two lines stand in a rowtwo pairs of pixels which adjoin over a sequence exist. The CFA pattern illustrated is based on the CFA pattern of the Bayer systemin the first sequenced and a green pixel are located in a line by turnsand a green and blue pixel is located in a line by turns in the following sequence. And it is arranged so that the green pixel of the continuing sequence may not adjoin the green pixel of a front sequence over a sequence. The structural layout of each pixel in each figure is the sameand the same element as the same position is arranged.

[0015]Probablyit will be clear that structure of each pixel of drawing 3 and drawing 4 approximates with a pixel shown in drawing 1 and drawing 2respectively. Therebya concept of this invention is compared with conventional technologyand it is explained clearly.

[0016]According to drawing 3the pixel architecture 20 is provided with the following.

The photodetector (PD) 22 which is either a photo-diode or a photogate.

Transfer gate (TG) 24.

Floating diffusion region (FD) 25.

A reset transistor including a reset gate (RG)the sequence selection transistor 28 containing the sequence selector gate (RSG) 29and the signal transistor (SIG) 21.

In the equipment of conventional technologyrespectivelyit is connected by bus for every pixel sequenceand the transfer gatereset gateand sequence selected node in 1 pixel are easy to carry out read-out by the row unit of a sensor. It startswhen the operation stop of the transfer gate is carried outand the storage period in the pixel of

the conventional technology of drawing 1 is ended when the transfer gate operates and an electric charge is transmitted to a floating diffusion region. Since all the transfer gates of each pixel within a predetermined sequence are connected by single bus the storage period of each pixel of the sequence is intrinsically the same.

[0017] According to the embodiment shown in drawing 3 the position of the transfer gate 24 is designed wire by the two individual transfer gate signal buses 1 and 2 or 3 and 4 in each sequence. According to this embodiment the green transfer gate (TGg) bus 1 and the red transfer gate (TGr) bus 2 are established in the sequence A and the TGg bus 3 and the blue transfer gate (TGb) bus 4 are established in the sequence B. The TGr bus 2 of the sequence A is electrically connected to each transfer gate 24 of the red pixel within the sequence A. The TGg bus 1 of the sequence A is electrically connected to all the transfer gates 24 of the green pixel within the sequence. It electrically connects with each transfer gate 24 of the green pixel within the sequence B and the TGg bus 3 of the sequence B electrically connects the TGb bus 4 of the sequence B to each transfer gate 24 of the blue pixel within the sequence B.

[0018] It explains below referring to drawing 11 with this one operational mode of a new architecture design to drawing 3. This mode is called focal plane shutter mode. An inventor thinks that its mode explained below is the optimal in this composition although it conceives of this composition shown in drawing 3 that it can be used in other modes. It is thought that red's sensitivity is the highest among the colors used within the pixel architecture 20 shown in drawing 3 and blue is considered that sensitivity is the lowest. An image sensor is initialized by operating before all the transfer gates 24 and reset gates are the time T_{1as} first shown in drawing 11. In order to start the storage period of the sequence A the operation stop of the TGg bus 1 is carried out and an electric charge is accumulated into the photodetector 22. This is simultaneously carried out by all the green pixels within the sequence A. After predetermined time carry out [the operation stop of the TGr bus 2] all the red pixels within the sequence A begin to accumulate an electric charge. At this time all the pixels within the sequence A are contained at the storage period. Desired period accumulation is carried out in the sequence A. In the meantime FD is reset and the sample of the reset level is carried out and it is held. Then TGr bus 2 and TGg bus 1 both operate

simultaneously and a signal charge is transmitted to a floating diffusion region. The sample of the signal level is carried out and it is held. Accumulation is carried out also in the sequence B during more than. First from the TGg bus 3 on sequence time when early the operation stop of the TGb bus 4 is carried out and the operation stop of a TGr bus continues after that. Then the sequence B is read like the sequence A. The above process is carried out in all the sequences of an image sensor. the timing of the tg with the same enforcement i.e. an odd number sequence -- the sequence A -- the same -- ***** is performed to the same timing as the sequence B. The relative storage time determined by the relative location of tg operation stop within sequence time is adjusted so that a desired color-balance may be obtained. The color with the lowest sensitivity has the longest storage time. That is it is programmed right [that]. Compared with it it is set up short appropriately and the storage time of other colors can also be set up by the ratio of the programmed longest storage time. Drawing 12 showed other operational modes of the equipment of drawing 3 and all the storage periods have lapped with the same time range there.

[0019] According to drawing 4 the pixel architecture 30 is provided with the following.

Usually the photodetector (PD) 32 which is a photo-diode.

A reset transistor including the reset gate (RG) 37.

The sequence selection transistor 38 containing a sequence selector gate (RSG).

Signal transistor (SIG) 31.

This is composition similar to the equipment of the conventional technology with same storage period of each pixel of a single tier shown in drawing 2. A storage period is until it reads from the time of the operation stop of the back reset gate where the photodetector was reset in the equipment of the conventional technology being carried out so that the electric charge in a photodetector may be read and a signal is impressed. Since the reset gate of each pixel within a predetermined sequence is connected by single bus the storage period of these pixels is intrinsically the same.

[0020] The embodiment shown in drawing 4 is designed so that the two individual reset gate buses 6 and 7 or 8 and 9 can wire each sequence. According to drawing 4 the sequence A is equipped with the green reset gate (RGg) bus 6 and the red reset gate (RGr) bus 7 and the sequence B is equipped with the RGg bus 8 and the blue reset gate (RGb) bus 9. The RGr bus 7 of the sequence A is electrically connected to the

reset gate 37 of all the red pixels within the sequence. The RGg bus 6 of the sequence A is electrically connected to the reset gate 37 of all the green pixels within the sequence. It electrically connects with the reset gate 37 of all the green pixels within the sequence B and the RGg bus 8 of the sequence B electrically connects the RGb bus 9 of the sequence B to the reset gate 37 of all the blue pixels within the sequence B.

[0021]The embodiment of drawing 4 has the same feature as the embodiment of drawing 3. However there is no transfer gate in the architecture of drawing 4 and it differs in that a storage period is set up using the reset gate 37. The kind of photodetector 32 to be used enables it to use the reset gate 37 for setting out of a storage period in the pixel architecture 30. The photodetector 32 is in the photo-diode and ***** containing both a standard photo-diode or the pin connection part 33 and the pin connectionless part 34 and by which pin connection was carried out selectively. Most photodetectors are the photo-diodes by which pin connection was carried out and it is formed of the pin connection part 33. The pin connectionless part 34 functions as a floating field used as an input node of the signal transistor 31.

[0022]Operation of the pixel architecture 30 is explained below referring to drawing 4. As well as having mentioned above about drawing 3 among the colors used within the pixel architecture 30 shown in drawing 4 it is thought that red's sensitivity is the highest and blue is considered that sensitivity is the lowest. An image sensor is initialized when the reset gate 37 operates. In order to start the storage period of the sequence A the operation stop of the RGg bus 6 is carried out and an electric charge is accumulated in the photodetector 32. This is simultaneously carried out by all the green pixels within the sequence A. After predetermined time carry out [the operation stop of the RGr bus 7] all the red pixels within the sequence A begin to accumulate an electric charge. In the sequence A desired period accumulation is carried out after that the sample of the signal level is carried out and it is held. Then the reset gate of the pixel of both colors operates and the sample of the reset level is carried out. Accumulation is carried out also in the sequence B during more than. First from the RGg bus 8 on sequence time when early the operation stop of the RGb bus 9 is carried out. Then the sequence B is read like the sequence A. The above process is carried out in all the sequences of an image sensor. the timing i.e. an odd number

sequence that the enforcement is the same -- the sequence A -- the same -- ***** is performed to the same timing as the sequence B. The relative storage time determined by the operation stop of the reset gate 37 within sequence time is adjusted so that a desired color-balance may be obtained. The color with the lowest sensitivity has the longest storage time. That is it is programmed right [that]. Compared with it it is set up short appropriately and the storage time of other colors can also be set up by the ratio of the programmed longest storage time.

[0023] Thus in the method of the electric charge dependence for planning a color-balance since accumulation of a noise electron is pressed down to the minimum the signal to noise ratio improves. The initial complement of signal processing which may make the fluctuation of substrate potential which makes a circuit noise increase and generates a pixel electronic noise induce is reduced.

[0024] The architecture of this invention provides the programmable color-balance achievement means characterized by use of an efficient silicon area and the high signal to noise ratio. In the CFA pattern of the Bayer system to illustrate the metallic line of 1 per single tier and an addition is required. In other CFA patterns the bus of many additions may be more nearly required than one per single tier. However in a CMOS (complementary metal oxide semiconductor) manufacturing process many metal layers are provided metal layers overlap mutually and can be arranged and since the transistor and gate of an addition in a pixel are unnecessary addition of one metal wire does not have an adverse effect on a filling factor. Since this architecture can be used with the present single amplifier read-out mechanism and the same pixel is used it is not generated by the image artifact resulting from the difference in an image sampling aperture. Some logic decoder circuits are needed per single tier. However since these are included in the CMOS logic besides an image array they do not have an adverse effect on a pixel and an image array field. The logic decoder circuit does not make an image processing signal circuit generate a noise in order to operate the whole sequence.

[0025] The concept of installing an individual transfer gate signal bus or a reset gate signal bus in each color is applicable also to the whole image array for every sequence as it was mentioned above. This application is preferred when a mechanical shutter reads it is closed down during a period and operation by frame imaging mode is easy.

[0026] The embodiment arranged by the straight line of this

invention is shown in drawing 5 in the Mie linear equipment (tri-linear device) 40. The timing chart for operation of this equipment is shown in drawing 13 and drawing 14. The Mie linear equipment 40 contains the linear sensors 8081 and 82. Each linear sensors 8081 and 82 are provided with the following.

The photodetector containing the photo-diode 42.

Transfer gate 43.

Floating diffusion region 44.

Each linear sensors 8081 and 82 have a sequence selector gate (RSG) a reset gate (RG) and the control circuit 45 containing a signal transistor (SIG). Here a light filter is provided in three pieces of the linear equipment 8081 and 82 respectively and it is set up so that the linear sensors 8081 and 82 may have sensitivity on red and green or blue wavelength. Each linear sensors 8081 and 82 are equipped with the individual transmission gate bus TGrTG and TGb at the important things respectively. Thereby an original storage period is individually controllable through a transmission gate bus for each linear sensors 8081 and 82.

[0027] Other embodiments arranged by the straight line of the active pixel sensor are shown in drawing 6. Including the individual linear sensors 8384 and 85 each linear sensor adjoins the reset gate 48 and the active pixel sensor 75 of this embodiment has the photo-diode 47 and also has the control circuit 49 containing a signal transistor (SIG) and a sequence selector gate (RSG). Like the embodiment of the above-mentioned linear equipment each linear sensors 8384 and 85 of drawing 6 are equipped with the individual reset gate bus RGrRG and RGb and the potential of these buses is controlled independently mutually. The reset gate bus RGrRG and RGb make possible individual reset control of each linear sensors 8384 and 85. It starts after reset of a pixel and the storage period of the linear sensor of drawing 6 continues until the electric charge accumulated into the photo-diode is detected by SIG. Therefore the individual reset gate bus RGrRG and RGb enable control which each linear sensors 8384 and 85 became independent of.

[0028] The active pixel sensor 50 of conventional technology is shown in drawing 7. This active pixel sensor contains the pixel which transmits an electric charge to the floating diffusion region 54 through the transfer gate 53 from the photogate 52 and which used the photogate 52 as the base. A storage period is determined to the timing which the photogate 52 is switched to discharge from accumulation and accumulation starts and the timing by which a photogate is continuously returned to accumulation and a

signal charge is transmitted to the floating diffusion region 54. If an electric charge is transmitted to the floating diffusion region 54 it will be detected by a reset gate (RG) a sequence selector gate (RSG) and the control circuit 55 containing a signal (SIG) transistor. A floating diffusion region functions as an input part to a SIG transistor. In the equipment of the conventional technology of drawing 7 in order to control the photogate 52 of each image sensor it has a single bus.

[0029] The active pixel sensor of other conventional technologies is shown in drawing 8. In this active pixel sensor transfer direct of the electric charge is carried out to the SIG transistor in the control circuit 59 from the photogate 57. Although the conventional technology equipment of above-mentioned drawing 7 and operation are similar a storage period is influenced by the time of the photogate 57 being switched to accumulation so that it may reset easily after read-out of a signal level here. Therefore a storage period is until a SIG transistor reads the charge level of the photogate 57 from the time of the pixel 56 being reset through the reset gate 58.

[0030] The embodiment of this invention which has an active pixel sensor based on the pixel architecture 60 is shown in drawing 9. In this active pixel sensor an electric charge is transmitted to the floating diffusion region 64 through the transfer gate 63 from the photogate 62. A storage period is determined to the timing which the photogate 62 is switched to discharge and accumulation starts and the timing by which a photogate is continuously returned to accumulation and a signal charge is transmitted to the floating diffusion region 64. If an electric charge is transmitted to the floating diffusion region 64 it will be detected by a reset gate (RG) a sequence selector gate (RSG) and the control circuit 65 containing a signal (SIG) transistor. A floating diffusion region functions as an input part to a SIG transistor.

[0031] The embodiment of this invention which has the active pixel sensor 70 using the pixel 71 which used the photogate as the base is shown in drawing 10. Here a storage period is influenced by the time of the photogate 72 being switched to accumulation so that it may reset easily after read-out of a signal level. Therefore from the time of a pixel being reset within the active pixel sensor 70 by a storage period's carrying out bias of the photogate 72 switching it to accumulation and transmitting an electric charge to the reset gate 73 It is until a SIG transistor reads the charge level of the photogate 72. The point that this invention

shown in drawing 10 differs from the pixel of the conventional technology of drawing 8 is a point which the individual bus PGrPGg and PGb are provided to redgreen and each blue and can control the photogate 72 of each color individually.

[0032] Drawing 11 is a timing chart showing operation with focal plane shutter mode in an array region shown in drawing 3. The length of each storage period is adjusted so that a suitable color-balance may be attained. tg expresses a storage period of a green pixel -- the sequence A and the sequence B -- it is alike respectively and carries out. tr expresses a storage period of a red pixel and is the shortest of the storage periods. tb expresses a storage period of a blue pixel -- a storage period -- it is the inner longest.

[0033] Drawing 12 is a timing chart showing operation with global shutter mode in an array region of this invention shown in drawing 3. A sign showing a storage period is the same as what was used by drawing 11. According to this chart storage time of each color is ended simultaneously. Thereby an image is simultaneously picturized by all the pixels. Although a pixel for a different color has a storage period of different length accumulation is carried out simultaneously. A storage period of the shortest color (red) is contained within a longer storage period of other channels.

[0034] Drawing 13 is a timing chart showing operation with focal plane shutter mode in the equipment arranged by the straight line of this invention shown in drawing 5. The storage period of a red channel is more nearly intentionally [than that of a green channel] short and the storage period of the green channel is intentionally shown short rather than that of the blue channel.

[0035] Drawing 14 is a timing chart showing operation with global shutter mode in the equipment arranged by the straight line of this invention shown in drawing 5. In this equipment accumulation of each pixel element in one color channels is carried out simultaneously. Although the channel for a different color has a storage period of different length accumulation is carried out simultaneously. Hereby starting and ending to different timing the storage period of each color channels is adjusted so that it may carry out when the central part of each storage period is the same. However centering of the storage period does not have to be carried out mutually in this way.

[0036] As far as an inventor gets to know the optimal mode for enforcement of this invention is explained by the above.

Clear modification of these modes is clear to a person skilled in the art and as it thinks best the range of this invention is judged according to a claim.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is a schematic illustration showing the APS pixel of conventional technology.

[Drawing 2] It is a schematic illustration showing other APS pixels of conventional technology.

[Drawing 3] It is a schematic illustration showing a first suitable embodiment of this invention.

[Drawing 4] It is a schematic illustration showing a first suitable embodiment of this invention.

[Drawing 5] It is a schematic illustration containing three linear sensors showing the embodiment which this invention arraigned linearly.

[Drawing 6] It is a schematic illustration showing the embodiment of everything but this invention arraigned linearly.

[Drawing 7] It is a schematic illustration using the pixel which used the photogate as the base showing the active pixel sensor of conventional technology.

[Drawing 8] It is a schematic illustration using the pixel which used the photogate as the base showing other active pixel sensors of conventional technology.

[Drawing 9] It is a schematic illustration containing the active pixel sensor using the pixel which used the photogate as the base showing the embodiment of this invention.

[Drawing 10] It is a schematic illustration containing the active pixel sensor using the pixel which used the photogate as the base showing the embodiment of this invention.

[Drawing 11] It is a timing chart showing operation with the focal plane shutter mode in the array region of this invention.

[Drawing 12] It is a timing chart showing operation with the global shutter mode in the array region of this invention.

[Drawing 13] It is a timing chart showing operation with the focal plane shutter mode in the linear equipment of this invention.

[Drawing 14] It is a timing chart showing operation with the global shutter mode in the linear equipment of this invention.

[Explanations of letters or numerals]

1 and 3 A green transfer gate (TGg) bus and 2 Red transfer gate (TGr) bus4 blue transfer gate (TGb) busand 6 and 8 Green reset gate (RGg) bus7 red reset gate (RGr) bus and 9 Blue reset gate (RGb) bus2030and 60 The pixel architecture2131 signal transistors22 and 32 A photodetector2443 and 5363 transfer gatesand 254454 and 64 Floating diffusion region374858and 73 A reset gatea 28 or 38-row selection transistor29 A sequence selector gate33 pin connection partsand 34 A pin connectionless part and 40 Mie linear equipment42 and 47 [A photogateand 56 and 71 / A pixeland 8081 828384 and 85 / Linear sensor.] A photo-diodeand 45495559 and 65 A control circuitand 5070 and 75 An active pixel sensorand 525762 and 72
